BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/961,229	09/20/2001	Vladimir Rumennik	003692P007XD4	4375

7590 08/20/2003

BRADLEY J. BEREZNAK
BURGESS & BEREZNAK, LLP
800 WEST EL CAMINO REAL
SUITE 180
MOUNTAIN VIEW, CA 94040

EXAMINER
HU, SHOUXIANG

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 08/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/961,229	RUMENNIK ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *50-57 and 93-111* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *50-57 and 93-111* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *10* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. This application is a divisional one of U.S. Serial No. 09/574,563, filed on 5/17/2000, which itself is a divisional one of 09/245,030, filed on 2/5/99, now U.S. Patent 6,207,994, which in turn is a continuation-in-part of U.S. Serial No. 08/744,182, filed on 11/5/96.

Pending Claims

2. Claims 50-57 and 93-111 are pending and remain active in this application.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7 of prior U.S. Patent No. 6,207,994 in view of Eklund (US 5,31,0982; of record).

Claims 50-57 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim1-7 of prior U.S. Patent No. 6,207,994. Although the conflicting claims are not identical, they are not patentably distinct from each other because they both claim the subject maters of an HVFET, comprising: a substrate of a first conductivity type; a source region of a second conductivity type disposed in the substrate, the source region having a source fingertip area; a first region of the second conductivity type disposed in the substrate spaced-apart from the source diffusion region with a channel region being formed therebetween, the first region being inter-digitated with the source region; a drain diffusion region of the second conductivity type disposed in the first region; a buffer area between the source diffusion region and the first region proximate the source region fingertip area, the buffer area being substantially wider than the channel region; an insulated gate disposed above the channel region; a plurality of buried layers of the first conductivity type disposed within the first region, the buried layers forming an associated plurality of JFET conduction channels in the first region, wherein the limitation of "a plurality of buried layers" is certainly readable as: comprising "a buried layer" in an open-ended manner; and that the "channel region" can be regarded as being formed of small channel regions.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 50-53 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Rumennik et al. ("Rumennik"; 5,258,636; of record) in view of Eklund (US 5,313,082; of record).

Rumennik disclose an HVFET (Figs. 3-5), comprising: a p-type substrate (68); an n-type source region (70) having a source fingertip area (54); an n-type first region (64) having a pair of drain fingertip areas inter-digitated with the source fingertip area; an isolated gate (56) above channel regions; an n-type drain diffusion region (74); a buffer area (near 54) wider than the channel regions; and, source and drain field plates (52 and 58).

Rumennik does not disclose that the first region can comprise a p-type buried layer. However, Eklund teach to form an HVFET (Fig. 1B; also see the abstract and col. 3, lines 1-62) having a p-type buried layer (27) within a first region (26) so as to form upper and lower JFET channels in the first region for reducing the on-resistance.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the p-type buried layer of Eklund into the HVFET of Rumennik, so that an HVFET with reduced on-resistance would be achieved.

Regarding claim 53, it is noted that having a well region connected to an external power supply through a tap diffusion region is one of the commonly used methods to adjust the potential of the well for achieving better potential match with other devices. It is therefore well within the ordinary skill in the art to incorporate a tap diffusion region near the edge of the first region in the above collectively taught HVFET, so that better potential match between devices would be achieved.

7. Claims 54 and 57 are further rejected under 35 U.S.C. 103(a) as being unpatentable over Rumennik in view of Eklund, as applied to claims 50-53, and further in view of Yamanishi et al. (JP404107877A).

The disclosures of Rumennik and Eklund are discussed as applied to claims 50-53 above.

Although Rumennik and Eklund do not expressly disclose that the buried layer can be spaced-apart from the drain diffusion region, Yamanishi teaches to form a HVFET (see Fig. 1, and the English abstract) having a p-type buried layer (10) formed in a first region (11) and spaced-apart from the drain diffusion region (9) for both of increasing the breakdown voltage and reducing the on-resistance.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above HVFET collectively taught by Rumennik and Eklund with the buried layer being spaced-apart from the drain diffusion region, as taught in Yamanishi, so that an HVFET with increased breakdown voltage and reduced on-resistance would be obtained.

Regarding claim 57, it is noted that Yamanishi further disclose that the buried p-type layer can be biased reversely to the drain area, and that it is art-known that a substrate can be commonly biased reversely to the drain region for achieving better device stability. Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to make the above collectively taught HVFET with the buried p-type layer being connected to the substrate, so that the p-type buried layer (s) would be desirably reversely biased.

8. Claims 55 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rumennik in view of Eklund, as applied to claims 50-53, and further in view of Williams (5,386,136; of record).

The disclosures of Rumennik and Eklund are discussed as applied to claims 50-53 above.

Although Rumennik and Eklund do not expressly disclose that the HVFET can further comprise a second p-type buried layer disposed beneath the source diffusion region and extended beneath the channel region, Williams teaches (Fig. 5) to form an HVFET having a second p-type buried layers (501, 503 and/or 504) buried beneath the source region (502) and extended beneath the channel region for increasing the breakdown voltage.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporate the second p-type layer of Williams into the

above collectively taught HVFET, so that an HVFET with increased breakdown voltage would be achieved.

9. Claims 93-95 and 99-111, insofar as being in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being obvious over Williams et al. ("Williams"; 5,386,136; of record) in view of Yamanishi et al. ("Yamanishi"; JP404107877A; of record) and/or Eklund (US 5,313,082; of record).

Williams discloses an HVFET (Fig. 4), comprising: a p-type substrate (205); an n-type epitaxial layer (206); a p-type diffusion region or first region (203 and a portion of 204), which inherently forms a junction with the surrounding n-type epitaxial layer (206); an n-type source diffusion region (202) with a source electrode (220); an isolated gate (209) above an IGFET channel region; an n-type drain region (207) with a drain electrode (208); an additional p-type buried region (201); and an additional p-type diffusion region or second region (the upper portion of 204).

Williams does not expressly disclose that the HVFET can further include a p-type buried layer in the n-type epitaxial layer between the channel and the drain so as to form current channels above and below the buried layer and that the current channel above the buried layer can have an impurity concentration of about $1x10^{12}/cm^2$.

However, one of ordinary skill in the art would readily recognize that the n-type epitaxial layer between channel and the drain in Williams inherently functions as an extended drain region therein. And, Yamanishi teaches to form an HVFET (see Fig. 1) with a p-type buried region (10) in an n-type extended drain region between (and

separated from the) channel and the drain for increasing the breakdown voltage and reducing the on-state resistance, wherein the buried region inherently functions as effective gate and is spaced-apart from the drain region. In addition, Eklund also teaches to form a buried layer to function as an effective gate so as to form current channels above and below the buried layer through appropriate doping control in the region above the buried layer (see the abstract and col. 3, lines 1-62) for reducing the on-resistance. It is further noted that, as also evidenced in Eklund (see col. 3, lines 43-62), the impurity concentration is an art-recognized parameter of importance subject to routine experimentation and optimization, and an impurity concentration of about $1x10^{12}/cm^2$ is well within the art-recognized range for a doping concentration of a JFET channel region.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to make the HVFET of Williams with a p-type-buried region being formed in the extended drain region and spaced-apart from the drain region and with the impurity concentration in the region above the buried layer being about $1x10^{12}/cm^2$, per the teachings of Yamanishi and/or Eklund, so that an HVFET with high breakdown voltage and low on-state resistance would be achieved.

Regarding claim 94, the buried layer in Yamanishi is spaced-apart from any junction.

Regarding claims 99 and 108, although Williams does not disclose that the buried region is connected to the substrate, Yamanishi further teaches that the buried p-type layer (10) can be biased reversely to the drain area (see the English Abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the HVFET taught by Williams in view of Yamanishi and/or Eklund above, with the buried region being connected to the substrate, so that the desirable reverse bias between the p-type buried region and the drain area would be obtained, per the further teaching of Yamanishi.

Regarding claim 111, one of ordinary skill in the art would readily recognize that field plate members can be desirably included in the source/drain electrode for further improving the breakdown voltage, as further evidenced in Yamanishi (see the expanded S/D electrodes (6 and 5 in Fig. 1).

10. Claims 96-98 are rejected under 35 U.S.C. 103(a) as being obvious over Williams in view of Yamanishi and/or Eklund, as applied to claims 93-95 and 99-111 above, and further in view of Colak (US 4,626,879).

The disclosures of Williams, Yamanishi and Eklund are discussed as applied to claims 93-95 and 99-111 above.

Although Williams, Yamanishi and Eklund do not expressly disclose that the p-type buried layer can overlap the gate and/or extend beneath the drain region, Colak teaches to form an HVFET (Fig. 1) having a p-type buried layer (16) overlapping the gate (30) and extending beneath the drain region (24), for improving the punchthrough and avalanche breakdown characteristics (see the abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the above HVFET taught by Williams in view of

Yamanishi and/or Eklund with the buried region overlapping the gate and extending beneath the drain region, as taught in Colak, so that an HVFET with improved punchthrough and avalanche breakdown characteristics would be obtained.

Response to Arguments

11. Applicant's arguments with respect to claims 50-57 and 93-111 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

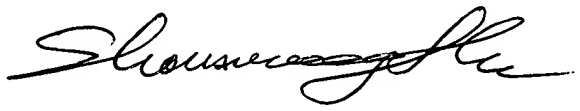
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is (703) 306-5729. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

SH
August 15, 2003



SHOUXIANG HU
PRIMARY EXAMINER